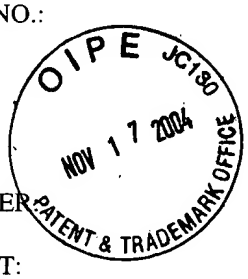
Attorney Docket: 00-332 / 1496.00075 AF IFW

IN RE APPLICATION OF: David Neil Pether et al.

RESPONSE TRANSMITTAL AND EXTENSION OF TIME REQUEST (IF REQUIRED)

SERIAL NO.: 09/739,956



TITLE: GENERATION OF GRAPHICS IN COMPUTER SYSTEMS

FILED: December 19, 2000

EXAMINER: Arnold, A.

ART UNIT: 2671

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Independent Claims	4 minus	4 =	0 x $ 88.00	$ 0.00
Multiple Dependent Claim First Added			+ $280.00	$ 0.00

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By: Jan M. Dunbar
Jan M. Dunbar

Our Docket No.: 00-332 / 1496.00075

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	David Neil Pether et al.		
Application No.:	09/739,956	Examiner:	Arnold, A.
Filed:	December 19, 2000	Art Group:	2697
For:	GENERATION OF GRAPHICS IN COMPUTER SYSTEMS		

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By: Jan M. Dunbar
Jan M. Dunbar

APPEAL BRIEF

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Dear Sir:

Appellants submit the following Appeal Brief pursuant to 37 C.F.R. §41.37 for consideration by the Board of Patent Appeals and Interferences. Please charge $340.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §41.20(b)(2) and any additional fees or credit any overpayment to Deposit Account Number 12-2252.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, LSI Logic Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 4-11, 13-21 and 23-30 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1, 4-11, 13-21 and 23-30.

IV. STATUS OF AMENDMENTS

Appellants are appealing an Office Action issued by the Examiner on June 18, 2004. On September 13, 2004, Appellants filed a Notice of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In a first embodiment (claim 1), the present invention concerns an apparatus (FIG. 2) for generating a region of graphics on a display. The apparatus generally comprises a bus (16, 22, 23), a plurality of registers (X24, Y26), a memory (14), a calculation circuit (30), a control circuit (36) and a clipping circuit (34).

The bus may have a first address range for the X and Y registers and a second address range for the memory. The memory may be directly connected to the bus and responsive within the second address range. The plurality of registers may reside within the first address range and be configured to store an X coordinate and a Y coordinate of a pixel to be drawn on a display. Access to the X and Y registers in the first address range is generally discussed on page 7, lines 19-26. Access to the memory is generally discusses on page 7, lines 1-6. Use of the registers is described on page 4, lines 6-11.

The calculation circuit may be configured to calculate an address in the second address range for storage of data corresponding to the pixel in dependence on the X and the Y coordinates as discussed on page 5, lines 13-18. The control circuit may configured to control writing of the data in the memory across the bus by driving the address onto the bus. Operation of the control circuit is generally described on page 6, lines 11-16, page 7, lines 7-14 and page 8, lines 7-24.

The clipping circuit may be configured for (i) comparing the X and the Y coordinates with predetermined clipping limits and (ii) generating a clipping signal configured to indicate that at least one of the X and the Y coordinates falls outside the predetermined clipping limits. Operation of the clipping circuit is generally described on page 5, line 28 thru page 6, line 16.

In a second embodiment (claim 15), the present invention concerns an apparatus (FIG. 2) for generating a region of graphics on a display. The apparatus generally comprises a register (24, 26), a calculation circuit (30), a control circuit (36), a bus (16, 22, 32) and a memory (14).

The register may be accessible via the bus for storing coordinates (X,Y) of a pixel to be drawn on the display. Access to the X and Y registers is generally discussed on page 7, lines 19-26.

The calculation circuit may be configured (i) for calculating an address in the memory directly connected to the bus for storage of data corresponding to the pixel in response to the coordinates and (ii) to output the address in a first part and a second part, the first part comprising a word address corresponding to the address in the memory and representing a single memory word and the second part comprising a bit address representing a position of the pixel data within the single memory word. Operation of the calculation circuit is generally discusses on page 5, lines 13-18 and page 14, line 25 thru page 15, line 16.

The control circuit may be configured for controlling the register and the calculation circuit to cause the data to be stored in the memory across the bus by driving the address onto the bus. Operation of the control circuit is generally described on page 6, lines 11-16, page 7, lines 7-14 and page 8, lines 7-24.

In a third embodiment (claim 20), the present invention concerns a method (operation of the apparatus in FIG. 2) of generating a region of graphics on a display. The method generally comprises the steps of storing an X coordinate (a first register 24), storing a Y coordinate (a second register 26), calculating an address (address convert 30), controlling writing (write control 36), memory mapping (CPU 12) the first register, memory mapping (CPU 12) the second register, a bus (16, 22, 32) and a memory (14).

Storing the X coordinate for a pixel to be drawn in a region may be performed in a first address range of the bus. Storing the Y coordinate for the pixel may be performed in the first address range. Access to the first and the second registers in the first address range is generally discussed on page 7, lines 19-26. Calculating an address in a second address range of the bus for storage of

data corresponding to the pixel in dependance on the X and the Y coordinates is generally described on page 5, lines 13-18.

Controlling writing of the data across the bus into the memory directly connected to the bus by driving the address onto the bus is discussed on page 6, lines 11-16, page 7, lines 7-14 and page 8, lines 7-24. Memory mapping a first register storing the X coordinate to a first location and a second location in the first address range and memory mapping a second register storing the Y coordinate to a third location and a fourth location in the first address range is generally covered on page 7, line 19 thru page 8, line 24.

In a fourth embodiment (claim 30), the present invention concerns an apparatus (FIG. 2) for generating a region of graphics on a display. The apparatus generally comprises a means for storing an X coordinate (an X register 24), a means for storing a Y coordinate (a Y register 26), a means for calculating an address (an address convert block 30), a means for controlling writing (a write control block 36), a bus (16, 22, 32) and a memory (14).

The means for storing the X coordinate for a pixel to be drawn in a region may be performed in a first address range of the bus. The means for storing the Y coordinate for the pixel may be performed in the first address range. Access to the X and the Y registers in the first address range is generally discussed on page 7, lines 19-26. The means for calculating an address in a second address range of the bus for storage of data corresponding to the pixel in dependance on the X and the Y coordinates is generally described on page 5, lines 13-18. The means for controlling writing of the data across the bus into the memory directly connected to the bus by driving the address onto the bus is discussed on page 6, lines 11-16, page 7, lines 7-14 and page 8, lines 7-24.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first issue is whether claims 1, 4-11, 13-21 and 23-30 are patentable under the 35 U.S.C. §112, first paragraph, written description criteria.

The second issue is whether claims 1, 4-7, 20, 21 and 30 are patentable under 35 U.S.C. §103(a) over Murphy, U.S. Patent No. 6,348,919.

The third issue is whether claims 15-19 and 27-29 are patentable under 35 U.S.C. §103(a) over Murphy in view of Ozcelik, U.S. Patent Publication No. 2002/0149626.

The fourth issue is whether claims 8-10 and 23-24 are patentable under 35 U.S.C. §103(a) over Murphy in view of Chiu, U.S. Patent No. 5,796,391.

The fifth issue is whether claim 14 is patentable under 35 U.S.C. §103(a) over Murphy and Prouty in further view of Chiu.

The sixth issue is whether claims 11, 13, 23 and 24 are patentable under 35 U.S.C. §103(a) over Murphy in view of Prouty.

VII. ARGUMENTS

A. 35 U.S.C. §112

1. Claims 1, 4-11, 13-21 and 23-30 are fully compliant with 35 U.S.C. §112, first paragraph, written description requirement.

The Examiner has stated, "Nowhere in the specification is there a description of a bus having a first address range and a second address range, where the X and Y registers are in the first range,

and the memory is in a second range."[1] In contrast, FIG. 2 of the application illustrates a graphics CPU 12 communicating on a system bus 16. Page 7, lines 1-4 of the application state:

> The X and Y coordinate values for each pixel are presented by the buffer 28 and applied to the ACCB 30. The ACCB 30 converts the pixel coordinates into a single number representative of an address in the system memory 14 using the following calculation:
>
> Address = Base + X + Y*Pitch

Page 1, lines 20-23 of the application provide an example in which pixel coordinates (X, Y) may range from (0, 0) to at least (4, 5). One of ordinary skill in the art would understand that the memory 14 on the system bus 16 has a second address range from at least an address(0, 0) = Base to at least an address (3, 4) = Base+3+4*Pitch. Therefore, the assertion by the Examiner that the specification fails to disclose a bus having a second address range is incorrect.

Furthermore, page 7, lines 19-26 of the application state:

> An improvement to the above-described operation of the pixel pipeline 20 is achieved by the use of double memory-mapping of each of the data registers 24,26. The registers 24,26 are memory-mapped and each is arranged to appear to the CPU 12 as two separate locations in memory each having a unique memory address. Thus the CPU 12 sees two possible X-registers at memory addresses N and N+1 and two Y-registers at memory addresses N+2 and N+3. These memory addresses need not be consecutive but are chosen so for convenience. In this example, memory address N to N+3 will generally be from 2000 to 2003 with addresses 200 and 2001 corresponding to the X-register 24 and addresses 2002 and 2003 representing the Y-register 26.

One of ordinary skill in the art would understand that the X register and the Y register reside in a first address range of the bus address space from at least an address 2000 to an address 2003. Therefore, the assertion by the Examiner that the specification does not describe a bus having a first address

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[1] Office Action, June 18, 2004, page 2, item 2.

range is incorrect. As such, the claims are fully compliant with the 35 U.S.C. §112, first paragraph, written description criteria and the rejection should be reversed.

B. Rejections under 35 U.S.C. § 103

The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness.[2] If the Examiner does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of non-obviousness.[3] "[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[4] "[T]he factual inquiry whether to combine references must be thorough and searching."[5] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[6] "It must be based on objective evidence of record."[7] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill

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[2] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Rev. 2, May 2004, §2142.

[3] *Id.*

[4] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[5] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[6] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[7] *Id.* at 1343, 61 USPQ2d at 1434.

in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations.[8]

The Federal Circuit has held that both the suggestion to modify or combine the references and the reasonable expectation of success must be found in the prior art itself, not merely in Appellant's disclosure.[9] Furthermore, the Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular."[10] Furthermore, the Board has held that the claimed invention is obvious only if either the references expressly or implicitly suggest the claimed invention, or **a convincing line of reasoning is presented by the examiner as to why an artisan would have found the claimed invention to be obvious in light of the teachings of the cited references.**[11]

As explained herein below, the Examiner has failed to establish a *prima facie* case of obviousness (i) because the cited references, alone or in combination, fail to teach or suggest all the elements of the presently claimed invention, (ii) because the Examiner has failed to provide a clear and particular suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify and/or combine the references and/or (iii) because the Examiner failed to put forth a convincing line of reasoning as to why an artisan would

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[8] M.P.E.P. §2142.

[9] See *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

[10] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999).

[11] See *Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985) (emphasis added by Appellant).

have found the claimed invention to be obvious in light of the teachings of the cited references.[12] As such, the presently pending claims are fully patentable over the cited references and the rejection should be reversed.

1. Rejection over Murphy

a. Claim 1 is fully patentable over Murphy.

Claim 1 provides (i) a bus having a first address range and a second address range and (ii) a plurality of registers within the first address range. The Examiner asserts that (i) a GLINT register file, as discussed in column 13, line 28 of Murphy, is similar to the claimed plurality of registers and (ii) FIG. 5C of Murphy illustrates a bus similar to the claimed bus.[13] Per column 13, lines 8-12 of Murphy, the GLINT register file is part of Region 0 of a PCI address map. The Host Bus in FIG. 5C of Murphy appears to be the only element capable of being a PCI bus. Therefore, the Examiner appears to assert that the Host Bus of Murphy is similar to the claimed bus.

Claim 1 provides a memory directly connected to the bus and responsive within the second address range. The Examiner asserts that an Output FIFO directly connected to a PCI bus in FIG. 2E of Murphy is similar to the claimed memory.[14]

Claim 1 further provides a calculation circuit configured to calculate an address in the second address range for storage of data corresponding to a pixel in dependence on the X and the Y

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[12] M.P.E.P. §2142.

[13] Office Action, June 18, 2004, page 3, item 1.

[14] Office Action, June 18, 2004, page 3, item 1.

coordinates. The Examiner asserts that a Graphics Hyperpipeline processor shown in FIG. 5C of Murphy calculates a local buffer address and thus is similar to the claimed control circuit.[15] In contrast, Murphy appears to be silent, and the Examiner offers no evidence or convincing line of reasoning how the Graphics Hyperpipeline processor (asserted similar to the claimed calculation circuit) calculates an address for the Output FIFO (asserted similar to the claimed memory) in the second address range of the PCI/Host bus (asserted similar to the claimed bus). Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations.

Claim 1 further provides a control circuit configured to control writing of data in a memory across the bus by driving an address onto the bus. The Examiner asserts that a Routing and Control block in FIG. 5D of Murphy is being similar to the claimed control circuit.[16] However, Murphy appears to be silent regarding the Routing and Control block (asserted similar to the claimed control circuit) writing data in the Output FIFO (asserted similar to the claims memory) across the PCI/Host bus (asserted similar to the claimed bus). As such, Murphy does not teach or suggest a control circuit configured to control writing of data in a memory across the bus by driving an address onto the bus as presently claimed.

Claim 1 further provides a clipping circuit configured to generate a clipping signal configured to indicate that at least one of the X and the Y coordinates falls outside predetermined clipping limits. The Examiner asserts that a clipping function defined by the Scissor Clip unit min and max

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[15] Office Action, June 18, 2004, page 3, item 1.

[16] See Amendment After Final, November 9, 2004, page 14, lines 6-8.

registers, as discussed in column 13, lines 39-41 of Murphy, is similar to the claimed clipping circuit.[17] In contrast, Murphy appears to be silent regarding the clipping function of the Scissor Clip registers generating a clipping signal that indicates that at least one of the Y and the Y coordinates predetermined clipping limits. Therefore, Murphy does not teach or suggest a clipping circuit configured to generate a clipping signal as presently claimed.

Furthermore, the Examiner argues that the Scissor Clip registers of Murphy can only be read if they generate a signal.[18] However, the Examiner's argument fails to address the signal being generated to indicate that at least one of the X and the Y coordinates falls outside predetermined clipping limits. Therefore, *prima facie* obviousness has not been established for lack of evidence that Murphy teaches or suggests all of the claim limitations.

In conclusion, the Examiner has failed to establish that Murphy teaches or suggest (i) a calculation circuit configured to calculate an address in a second address range for storage of data corresponding to a pixel in dependence on an X and a Y coordinates, (ii) a control circuit configured to control writing of data in a memory across a bus by driving an address onto the bus and (iii) a clipping circuit configured to generate a clipping signal configured to indicate that at least one of the X and the Y coordinates falls outside predetermined clipping limits. As such, the rejection of claim 1 over the cited reference should be reversed.

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[17] Office Action, June 18, 2004, page 4, item 1.

[18] Office Action, June 18, 2004, page 9, last line to page 10, second line.

b. Claim 20 is fully patentable over Murphy.

Claim 20 provides steps for (A) storing an X coordinate for a pixel to be drawn in a region of a graphics (on a display) in a first address range of a bus and (B) storing a Y coordinate for the pixel in the first address range. The Examiner asserts that claim 20 is rejected for the same reason as claims 1 and 7.[19] The Examiner apparently asserts that (i) a GLINT register file, as discussed in column 13, line 28 of Murphy, is similar to the claimed storing steps and (ii) FIG. 5C of Murphy illustrates a bus similar to the claimed bus.[20] Per column 13, lines 8-12 of Murphy, the GLINT register file is part of Region 0 of a PCI address map. The Host Bus in FIG. 5C of Murphy appears to be the only element capable of being a PCI bus. Therefore, the Examiner appears to assert that the Host Bus of Murphy is similar to the claimed bus.

Claim 20 provides (in step D) a memory directly connected to the bus. The Examiner asserts that an Output FIFO directly connected to a PCI bus in FIG. 2E of Murphy is similar to the claimed memory.[21]

Claim 20 further provides a step for (C) calculating an address in a second address range of the bus for storage of the data corresponding to the pixel in dependance on the X and the Y coordinates. The Examiner asserts that a Graphics Hyperpipeline processor shown in FIG. 5C of Murphy calculates a local buffer address and thus is similar to the claimed control circuit.[22] In

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[19] Office Action, June 18, 2004, page 5, first paragraph.

[20] Office Action, June 18, 2004, page 3, item 1.

[21] Office Action, June 18, 2004, page 3, item 1.

[22] Office Action, June 18, 2004, page 3, item 1.

contrast, Murphy appears to be silent, and the Examiner offers no evidence or conclusive line of reasoning how the Graphics Hyperpipeline processor (asserted similar to the claimed calculation circuit) calculates an address for the Output FIFO (asserted similar to the claimed memory) in the second address range of the PCI/Host bus (asserted similar to the claimed bus). Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations.

Claim 20 further provides a step for (D) controlling writing of data across the bus into the memory directly connected to the bus by driving the address onto the bus. The Examiner asserts that a Routing and Control block in FIG. 5D of Murphy is being similar to the claimed controlling step.[23] However, Murphy appears to be silent regarding the Routing and Control block (asserted similar to the claimed controlling step) writing data in the Output FIFO (asserted similar to the claimed memory) across the PCI/Host bus (asserted similar to the claimed bus). As such, Murphy does not teach or suggest a step for controlling writing of data across a bus into a memory directly connected to the bus by driving an address onto the bus as presently claimed.

Claim 20 further provides steps for (E) memory mapping a first register storing an X coordinate to a first location and a second location in a first address range and (F) memory mapping a second register storing a Y coordinate to a third location and a fourth location in the first address range. The Examiner asserts that Murphy teaches that each of the GLINT registers is 4 bytes wide and that each byte is at a different address.[24] The text of Murphy cited by Examiner states:

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[23] See Amendment After Final, November 9, 2004, page 14, lines 6-8.

[24] Office Action, June 18, 2004, page 4, last paragraph.

> When a GLINT host software driver is initialized it can map the register file into its address space. Each register has an associated address tag, giving its offset from the base of the register file (since all registers reside on a 64-bit boundary, the tag offset is measured in multiples of 8 bytes).
> ...
> The last write triggers the start of rendering. GLINT has approximately 200 registers.

Nowhere in the above text does Murphy appear to discuss a register memory mapped to two locations. Furthermore, the Examiner's assertion that each register of Murphy has 4 bytes in different locations is moot since the 4 bytes are still within a single register and appear to be accessed at a single address determined by the tag offset. Therefore, the Examiner has failed to establish that Murphy teaches or suggests steps for (i) memory mapping a first register storing an X coordinate to a first location and a second location in a first address range and (ii) memory mapping a second register storing a Y coordinate to a third location and a fourth location in the first address range as presently claimed.

In conclusion, the Examiner has failed to establish that Murphy teaches or suggest (i) a step for calculating an address in a second address range of a bus for storage of data corresponding to a pixel in dependance on an X and a Y coordinates, (ii) a step for controlling writing of data across the bus into the memory directly connected to the bus by driving the address onto the bus, (iii) memory mapping a first register storing the X coordinate to a first location and a second location in a first address range and (iv) memory mapping a second register storing the Y coordinate to a third location and a fourth location in the first address range. As such, the rejection of claim 20 over the cited reference should be reversed.

c. Claim 30 is fully patentable over Murphy.

Claim 30 provides (i) a means for storing an X coordinate for a pixel to be drawn in a region of a graphics (on a display) in a first address range of a bus and (ii) a means for storing a Y coordinate for the pixel in the first address range. The Examiner asserts that claim 30 is rejected for the same reason as claim 1.[25] The Examiner asserts that (i) a GLINT register file, as discussed in column 13, line 28 of Murphy, is similar to the two claimed means for storing and (ii) FIG. 5C of Murphy illustrates a bus similar to the claimed bus.[26] Per column 13, lines 8-12 of Murphy, the GLINT register file is part of Region 0 of a PCI address map. The Host Bus in FIG. 5C of Murphy appears to be the only element capable of being a PCI bus. Therefore, the Examiner appears to assert that the Host Bus of Murphy is similar to the claimed bus.

Claim 30 provides (in a fourth means) a memory directly connected to the bus. The Examiner asserts that an Output FIFO directly connected to a PCI bus in FIG. 2E of Murphy is similar to the claimed memory.[27]

Claim 30 further provides a means for calculating an address in a second address range of the bus for storage of the data corresponding to the pixel in dependance on the X and the Y coordinates. The Examiner asserts that a Graphics Hyperpipeline processor shown in FIG. 5C of Murphy calculates a local buffer address and thus is similar to the claimed control circuit.[28] In

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[25] Office Action, June 18, 2004, page 5, third paragraph.

[26] Office Action, June 18, 2004, page 3, item 1.

[27] Office Action, June 18, 2004, page 3, item 1.

[28] Office Action, June 18, 2004, page 3, item 1.

contrast, Murphy appears to be silent, and the Examiner offers no evidence or conclusive line of reasoning how the Graphics Hyperpipeline processor (asserted similar to the claimed calculation circuit) calculates an address for the Output FIFO (asserted similar to the claimed memory) in the second address range of the PCI/Host bus (asserted similar to the claimed bus). Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations.

Claim 30 further provides a means for controlling writing of data across the bus into the memory directly connected to the bus by driving the address onto the bus. The Examiner asserts that a Routing and Control block in FIG. 5D of Murphy is being similar to the claimed controlling step.[29] However, Murphy appears to be silent regarding the Routing and Control block (asserted similar to the claimed controlling step) writing data in the Output FIFO (asserted similar to the claimed memory) across the PCI/Host bus (asserted similar to the claimed bus). As such, Murphy does not teach or suggest a means for controlling writing of data across a bus into a memory directly connected to the bus by driving an address onto the bus as presently claimed.

In conclusion, the Examiner has failed to establish that Murphy teaches or suggest (i) a means for calculating an address in a second address range of a bus for storage of data corresponding to a pixel in dependance on an X and a Y coordinates and (ii) a means for controlling writing of data across the bus into the memory directly connected to the bus by driving the address onto the bus. As such, the rejection of claim 30 over the cited reference should be reversed.

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[29] See Amendment After Final, November 9, 2004, page 14, lines 6-8.

d. Claim 4 is fully patentable over Murphy.

Claim 4 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 4.

Claim 4 further provides that the control circuit is configured to inhibit writing of data to an address in response to a clipping signal. In contrast, the Examiner admits that Murphy does not teach inhibiting writing.[30] Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning for (i) modifying the Scissor Clip registers of Murphy (asserted similar to the claimed clipping circuit) to generate a clipping signal and (ii) modifying the Routing and Control block of Murphy (asserted similar to the claimed control circuit) to inhibit writing of data to the Output FIFO of Murphy (asserted similar to the claimed memory) in response to the clipping signal. Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations.

Furthermore, the Examiner asserts that pixels outside a range "are extraneous and no further processing will be carried out on them."[31] However, the Examiner provides no evidence that the assertion is true. Therefore, the Examiner's assertion should be disregarded as merely a conclusory statement. As such, the rejection of claim 4 over the cited reference should be reversed.

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[30] Office Action, June 18, 2004, page 4, second paragraph.

[31] Office Action, June 18, 2004, page 4, second paragraph.

e. Claim 5 is fully patentable over Murphy.

Claim 5 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 5.

Claim 5 further provides that the control circuit is further configured to prevent calculation of the address in response to the clipping signal. The Examiner asserts that claim 5 is rejected for the same reasons as claim 4.[32] However, nowhere in the rejection of claim 4 does the Examiner discuss the Routing and Control block of Murphy (asserted similar to the claimed control circuit) not calculating an address in response to a clipping signal. Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations. As such, the rejection of claim 5 over the cited reference should be reversed.

f. Claim 6 is fully patentable over Murphy.

Claim 6 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 6.

Claim 6 further provides that data is discarded when at least one of the X and the Y coordinates fall outside the predetermined clipping limits. The Examiner asserts that claim 6 is rejected for the same reasons as claim 4.[33] However, nowhere in the rejection of claim 4 does the

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[32] Office Action, June 18, 2004, page 4, third paragraph.

[33] Office Action, June 18, 2004, page 4, fourth paragraph.

Examiner discuss discarding data. Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations. As such, the rejection of claim 6 over the cited reference should be reversed.

g. Claim 7 is fully patentable over Murphy.

Claim 7 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 7.

Claim 7 further provides (i) a first register of the plurality of registers is memory mapped to a first location and a second location in the first address range and (ii) a second register of the plurality of registers is memory mapped to a third location and a fourth location in the first memory range. The Examiner asserts that Murphy teaches that each of the GLINT registers is 4 bytes wide and that each byte is at a different address.[34] The text of Murphy cited by Examiner states:

> When a GLINT host software driver is initialized it can map the register file into its address space. Each register has an associated address tag, giving its offset from the base of the register file (since all registers reside on a 64-bit boundary, the tag offset is measured in multiples of 8 bytes).
> ...
> The last write triggers the start of rendering. GLINT has approximately 200 registers.

Nowhere in the above text does Murphy appear to discuss a register memory mapped to two locations. Furthermore, the Examiner's assertion that each register of Murphy has 4 bytes in different locations is moot since the 4 bytes are still within a single register and appear to be accessed at a single address determined by the tag offset. Therefore, the Examiner has failed to establish that

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[34] Office Action, June 18, 2004, page 4, last paragraph.

Murphy teaches or suggests (i) a first register of the plurality of registers is memory mapped to a first location and a second location in the first address range and (ii) a second register of the plurality of registers is memory mapped to a third location and a fourth location in the first memory range as presently claimed. As such, the rejection of claim 7 over the cited reference should be reversed.

h. Claim 21 is fully patentable over Murphy.

Claim 21 depends from claim 20 and thus contains all of the limitations of claim 20. Consequently, the arguments presented above in support of the patentability of claim 20 are incorporated hereunder in support of claim 21.

Claim 21 further provides a step for discarding data when at least one of the X and the Y coordinates fall outside the predetermined clipping limits. The Examiner asserts that claim 21 is rejected for the same reasons as claim 4.[35] However, nowhere in the rejection of claim 4 does the Examiner discuss discarding data. Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence that Murphy teaches or suggests all of the claim limitations. As such, the rejection of claim 21 over the cited reference should be reversed.

2. Rejection over Murphy in view of Ozcelik

a. Claim 15 is fully patentable over Murphy and Ozcelik.

Claim 15 provides a register accessible via a bus for storing coordinates of a pixel to be drawn on a display. In contrast, the Examiner provides no evidence or arguments that Murphy

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[35] Office Action, June 18, 2004, page 5, second paragraph.

and/or Ozcelik teach or suggest a register accessible via a bus for storing coordinates of a pixel to be drawn on a display as presently claimed. Therefore, *prima facie* obviousness has not been established.

Claim 15 further provides a calculation circuit for calculating an address in a memory directly connected to the bus for storage of data corresponding to the pixel in response to the coordinates. In contrast, the Examiner provides no evidence or arguments that Murphy and/or Ozcelik teach or suggest a calculation circuit for calculating an address in a memory directly connected to the bus for storage of data corresponding to the pixel in response to the coordinates as presently claimed. Therefore, *prima facie* obviousness has not been established.

Claim 15 further provides a control circuit for controlling the register and the calculation circuit to cause the data to be stored in the memory across the bus by driving the address onto the bus. In contrast, the Examiner provided no evidence or arguments that Murphy and/or Ozcelik teach or suggest a control circuit for controlling the register and the calculation circuit to cause the data to be stored in the memory across the bus by driving the address onto the bus as presently claimed. Therefore, *prima facie* obviousness has not been established.

Furthermore, the Examiner has not established motivation to combine Murphy and Ozcelik. The Examiner asserts that motivation exists "to consume less storage space. See Ozcelik, paragraph 4."[36] The text cited by the Examiner reads:

> [0004] Unfortunately, there is a penalty associated with producing rich on-screen display environments; specifically, the complexity of the hardware needed to support such displays is substantial. Typically a graphic display is produced by providing to hardware a palette of luminance and/or color values and a bit map of values for each pixel in a region of the

[36] Office Action, June 18, 2004, page 8, top paragraph.

> display. The values are used to look up luminance and color values for each pixel and display the pixel on the screen. To achieve a reasonable color depth necessary for pleasing icons, the size of the palette may become quite large, and as a result, consume substantial storage space. Furthermore, to display different icons or different graphics in different areas of the display, different palettes may be required.

Nowhere in the above text does Ozcelik appear to discuss consuming less space, as asserted by the Examiner. Therefore, the asserted motivation is merely a conclusory statement. As such, *prima facie* obviousness has not been established for lack of motivation to combine the references.

In conclusion, the Examiner has failed to establish that Murphy and Ozcelik, alone or in combination, teach or suggest (i) a register accessible via a bus for storing coordinates of a pixel to be drawn on a display, (ii) a calculation circuit for calculating an address in a memory directly connected to the bus for storage of data corresponding to the pixel in response to the coordinates and (iii) a control circuit for controlling the register and the calculation circuit to cause the data to be stored in the memory across the bus by driving the address onto the bus. Furthermore, motivation to combine the references has not been established. As such, the rejection of claim 15 over the cited references should be reversed.

b. Claim 16 is fully patentable over Murphy and Ozcelik.

Claim 16 depends from claim 15 and thus contains all of the limitations of claim 15. Consequently, the arguments presented above in support of the patentability of claim 15 are incorporated hereunder in support of claim 16.

Claim 16 further provides a second register for storing pixel data in a single memory word prior to the single memory word being written to the address in the memory. Despite the assertion

by the Examiner[37], column 16, lines 15-16 of Murphy appear to be silent regarding a register for storing pixel data in a single work memory prior to the single memory word being written to an address in a memory. The cited test of Murphy reads:

> For example, this is useful for image download where pixel data is continuously written to the Color register.

Nowhere in the above text does Murphy discuss the Color register storing pixel data in a single memory word prior to the single memory word being written to an address in a memory. Therefore, *prima facie* obviousness has not been established for lack of evidence that Murphy and/or Ozcelik teach or suggest all of the claim limitations.

Claim 16 further provides a logic unit for writing data to the second register in dependence on the address calculated by the calculation circuit. Despite the assertion by the Examiner,[38] a multiplexer in FIG. 2B of Murphy does not appear to be a logic unit writing data to a register. Murphy appears to be silent regarding the multiplexer writing in dependence on an address calculated by the Graphics Hyperpipline block (asserted similar to the claimed calculation circuit in the other independent claim rejections). Therefore, Murphy and Ozcelik, alone or in combination, do not teach or suggest a logic unit for writing data to the second register in dependence on the address calculated by the calculation circuit as presently claimed. As such, the rejection of claim 16 over the cited references should be reversed.

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[37] Office Action, June 18, 2004, page 8, second paragraph.

[38] Office Action, June 18, 2004, page 8, second paragraph.

c. Claim 17 is fully patentable over Murphy and Ozcelik.

Claim 17 depends from claim 16 and thus contains all of the limitations of claim 16. Consequently, the arguments presented above in support of the patentability of claim 16 are incorporated hereunder in support of claim 17.

Claim 17 further provides that the logic unit combines data for at least two pixels to be drawn in dependence on the address of each of pixel to permit storage of the data for the pixels in the single memory word. In contrast, the Examiner asserts that modifying a multiplexer to combine data for two or more pixels would be obvious.[39] However, no evidence or convincing line of reasoning is provided why modifying a multiplexer to perform a non-multiplexing function would be obvious. Therefore, the Examiner's assertion is merely a conclusory statement and thus *prima facie* obviousness has not been established. As such, the rejection of claim 17 over the cited references should be reversed.

d. Claim 18 is fully patentable over Murphy and Ozcelik.

Claim 18 depends from claim 17 and thus contains all of the limitations of claim 17. Consequently, the arguments presented above in support of the patentability of claim 17 are incorporated hereunder in support of claim 18.

Claim 18 further provides a comparator connected to the calculation circuit for (i) receiving the addresses, (ii) comparing the addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if the addresses are identical. In contrast, the Examiner asserts that it would

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[39] Office Action, June 18, 2004, page 8, third paragraph.

have been obvious to modify Murphy and Ozcelik to add an address comparison operation.[40] Alleged motivation is that "comparison operations are frequently used in graphics processing to preserve physical memory."[41] However, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[42] Furthermore, no evidence or convincing line of reasoning is provided why comparing two pixel addresses results in a preservation of physical memory. Therefore, *prima facie* obviousness has not been established for lack of motivation to modify the references.

e. Claim 19 is fully patentable over Murphy and Ozcelik.

Claim 19 depends from claim 18 and thus contains all of the limitations of claim 18. Consequently, the arguments presented above in support of the patentability of claim 18 are incorporated hereunder in support of claim 19.

Claim 19 further provides that the control circuit is further configured to combine data for pixels in response to a receipt of the same address signal. In contrast, the Examiner admits that Murphy "does not disclose comparing address of pixels to be drawn."[43] Therefore, the assertion that Murphy teaches combining pixel data when the addresses are the same conflicts the Examiner's own admission that no such address comparison is done. Therefore, *prima facie* obviousness has not

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[40] Office Action, June 18, 2004, page 8, last two lines.

[41] Office Action, June 18, 2004, page 9, lines 1-2.

[42] M.P.E.P. §2143.01

[43] Office Action, June 18, 2004, page 8, last three lines.

been established for lack of evidence that Murphy and/or Ozcelik teach or suggest all of the claim limitations. As such, the rejection of claim 19 over the cited references should be reversed.

f. Claim 27 is fully patentable over Murphy and Ozcelik.

Claim 27 depends from claim 20 and thus contains all of the limitations of claim 20. Consequently, the arguments presented above in support of the patentability of claim 20 are incorporated hereunder in support of claim 27.

Claim 27 further provides a step for storing data in a single memory word prior to the single memory word being written to the address in the memory in dependence on the word address or a bit address. The Examiner asserts that claim 27 is rejected for the same reasons as claims 17 and 20.[44] However, none of the rejection arguments for claims 17 and/or 20 discuss a step for storing data in a single memory word prior to the single memory word being written to the address in the memory in dependence on the word address or a bit address as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection of claim 27 over the cited references should be reversed.

g. Claim 28 is fully patentable over Murphy and Ozcelik.

Claim 28 depends from claim 20 and thus contains all of the limitations of claim 20. Consequently, the arguments presented above in support of the patentability of claim 20 are incorporated hereunder in support of claim 28.

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[44] Office Action, June 18, 2004, page 9, third paragraph.

Claim 28 further provides a step for combining data for at least two pixels to be drawn in dependence on a word address of each of the pixels to permit storage of data for the pixels in a single memory word. The Examiner asserts that claim 28 is rejected for the same reason as claims 15 and 20.[45] However, none of the rejection arguments for claims 15 and/or 20 discuss a step for combining data for at least two pixels to be drawn in dependence on a word address of each of the pixels to permit storage of data for the pixels in a single memory word as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection of claim 28 over the cited references should be reversed.

h. Claim 29 is fully patentable over Murphy and Ozcelik.

Claim 29 depends from claim 28 and thus contains all of the limitations of claim 28. Consequently, the arguments presented above in support of the patentability of claim 28 are incorporated hereunder in support of claim 29.

Claim 29 further provides steps for (i) comparing the word address of consecutive pixels to be drawn and (ii) combining data for the pixels if the word addresses are identical. The Examiner asserts that claim 29 is rejected for the same reason as claims 18 and 20. However, none of the rejection arguments for claims 18 and/or 20 discuss steps for (i) comparing the word address of consecutive pixels to be drawn and (ii) combining data for the pixels if the word addresses are identical as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection of claim 29 over the cited references should be reversed.

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[45] Office Action, June 18, 2004, page 9, fourth paragraph.

3. Rejection over Murphy in view of Chiu

a. Claim 8 is fully patentable over Murphy and Chiu.

Claim 8 depends from claim 7 and thus contains all of the limitations of claim 7. Consequently, the arguments presented above in support of the patentability of claim 7 are incorporated hereunder in support of claim 8.

Claim 8 further provides an address decoder for (i) monitoring a first, a second, a third and a fourth memory locations and (ii) applying a location signal to a control circuit representative of an address location being written to. In contrast, Murphy and Chiu each appear to be silent regarding a circuit that both monitors multiple locations and generates a signal representative of which of the multiple locations is being written to. Furthermore, a control signal associated with the address decoder 206 of Chiu appears to be an input received by the address decoder 206, not an output signal applied by the address decoder 206 to another circuit. Therefore, Murphy and Chiu, alone or in combination, do not appear to teach or suggest an address decoder for (i) monitoring a first, a second, a third and a fourth memory locations and (ii) applying a location signal to a control circuit representative of an address location being written to as presently claimed.

Furthermore, the Examiner does not provide any evidence of motivation from either the references or knowledge generally available to one of ordinary skill in the art to modify or combine the references. In particular, the Examiner improperly credits motivation to the teachings of the appellants.[46] Therefore, *prima facie* obviousness has not been established for lack of motivation to

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[46] Office Action, June 18, 2004, page 5, item 2.

modify or combine the references. As such, the rejection of claim 8 over the cited references should be reversed.

b. Claim 9 is fully patentable over Murphy and Chiu.

Claim 9 depends from claim 8 and thus contains all of the limitations of claim 8. Consequently, the arguments presented above in support of the patentability of claim 8 are incorporated hereunder in support of claim 9.

Claim 9 further provides that the control circuit is configured to control the first and the second registers and the calculation circuit in response to the location signal. The Examiner asserts that claim 9 is rejected for the same reasons as claims 1 and 8.[47] However, none of the rejection arguments for claims 1 and/or 8 discuss the control circuit configured to control the first and the second registers and the calculation circuit in response to the location signal as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection of claim 9 over the cited references should be reversed.

c. Claim 10 is fully patentable over Murphy and Chiu.

Claim 10 depends from claim 9 and thus contains all of the limitations of claim 9. Consequently, the arguments presented above in support of the patentability of claim 9 are incorporated hereunder in support of claim 10.

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[47] Office Action, June 18, 2004, page 5, last paragraph.

Claim 10 further provides that the control circuit is further configured is further configured to instruct the calculate circuit to calculate the address in response to one of the following (i) the X coordinate being written to a preselected one of the first and the second locations and (ii) the Y coordinate being written to a preselected one of the third and the fourth locations. The Examiner asserts that claim 10 is rejected for the same reasons as claims 1 and 8.[48] However, none of the rejection arguments for claims 1 and/or 8 discuss the control circuit configured is further configured to instruct the calculate circuit to calculate the address in response to one of the following (i) the X coordinate being written to a preselected one of the first and the second locations and (ii) the Y coordinate being written to a preselected one of the third and the fourth locations as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection of claim 10 over the cited references should be reversed.

d. Claim 23 is fully patentable over Murphy and Chiu.

Claim 23 depends from claim 20 and thus contains all of the limitations of claim 20. Consequently, the arguments presented above in support of the patentability of claim 20 are incorporated hereunder in support of claim 23.

Claim 23 further provides a step for monitoring the first, the second, the third and the fourth locations for a write. The Examiner asserts that claim 23 is rejected for the same reasons as claim 8 and 22.[49] However, none of the arguments in the rejection for claim 8 discuss a step for monitoring

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[48] Office Action, June 18, 2004, page 6, first paragraph.

[49] Office Action, June 18, 2004, page 6, second paragraph.

the first, the second, the third and the fourth locations for a write as presently claimed. Furthermore, claim 22 was previously cancelled and thus has no rejection arguments. As such, *prima facie* obviousness has not been established.

Furthermore, the Examiner does not provide any evidence of motivation from either the references or knowledge generally available to one of ordinary skill in the art to modify or combine the references. In particular, the Examiner improperly credits motivation to the teachings of the appellants.[50] Therefore, *prima facie* obviousness has not been established for lack of motivation to modify or combine the references. As such, the rejection of claim 23 over the cited references should be reversed.

e. Claim 24 is fully patentable over Murphy and Chiu.

Claim 24 depends from claim 20 and thus contains all of the limitations of claim 20. Consequently, the arguments presented above in support of the patentability of claim 20 are incorporated hereunder in support of claim 24.

Claim 24 further provides a step for calculating the address for a pixel in response to one of the following (i) the X coordinate being written to a preselected one of the first and the second locations and (ii) the Y coordinate being written to a preselected one of the third and the fourth locations. The Examiner asserts that claim 24 is rejected for the same reasons as claim 8 and 22.[51] However, none of the rejection arguments for claim 8 discuss a step for calculating the address for

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[50] Office Action, June 18, 2004, page 5, item 2.

[51] Office Action, June 18, 2004, page 6, third paragraph.

a pixel in response to one of the following (i) the X coordinate being written to a preselected one of the first and the second locations and (ii) the Y coordinate being written to a preselected one of the third and the fourth locations as presently claimed. Furthermore, claim 22 was previously cancelled and thus has no rejection arguments. Therefore, *prima facie* obviousness has not been established and the rejection of claim 23 over the cited references should be reversed.

4. Rejection over Murphy in view of Prouty and Chiu

a. Claim 14 is fully patentable over Murphy, Prouty and Chiu.

Claim 14 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 14.

Claim 14 further provides an address decoder for indexing a style counter in response to an address location being written to. The Examiner asserts that claim 14 is rejected for the same reasons as claims 8 and 11. However, none of the rejection arguments for claims 8 and/or 11 discuss the address decoder indexing a style counter in response to and address location being written to as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection of claim 14 over the cited references should be reversed.

5. Rejection over Murphy in view of Prouty

a. Claims 11 and 13 fully patentable over Murphy and Prouty.

Claims 11 and 13 depend from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claims 11 and 13.

b. Claims 25 and 26 fully patentable over Murphy and Prouty.

Claims 25 and 26 depend from claim 20 and thus contains all of the limitations of claim 20. Consequently, the arguments presented above in support of the patentability of claim 20 are incorporated hereunder in support of claims 25 and 26.

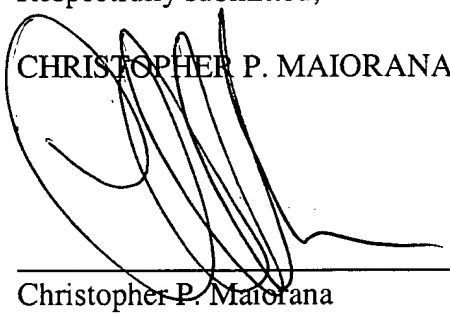
C. CONCLUSION

None of the cited references, alone or in combination, teach or suggest an apparatus and/or method for generating a region of graphics on a display as presently claimed. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited references. However, should the Board find the

arguments herein in support of independent claims 1, 15, 20 and/or 30 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable claims.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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VIII. CLAIM APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a bus having a first address range and a second address range;

a plurality of registers within said first address range configured to store an X coordinate and a Y coordinate of a pixel to be drawn on said display;

a memory directly connected to said bus and responsive within said second address range;

a calculation circuit configured to calculate an address in said second address range for storage of data corresponding to said pixel in dependence on said X and said Y coordinates;

a control circuit configured to control writing of said data in said memory across said bus by driving said address onto said bus; and

a clipping circuit for (i) comparing said X and said Y coordinates with predetermined clipping limits and (ii) generating a clipping signal configured to indicate that at least one of said X and said Y coordinates falls outside said predetermined clipping limits.

2. (CANCELED)

3. (CANCELED)

4. The apparatus as claimed in claim 3, wherein said control circuit is further configured to inhibit writing of said data to said address in response to said clipping signal.

5. The apparatus as claimed in claim 3, wherein said control circuit is further configured to prevent calculation of said address in response to said clipping signal.

6. The apparatus as claimed in claim 3, wherein said data is discarded when at least one of said X and said Y coordinates fall outside said predetermined clipping limits.

7. The apparatus as claimed in claim 1, wherein (i) a first register of said registers is memory mapped to a first location and a second location in said first address range and (ii) a second register of said registers is memory mapped to a third location and a fourth location in said first memory range.

8. The apparatus as claimed in claim 7, wherein said apparatus further comprises:

an address decoder for (i) monitoring said first, said second, said third and said fourth memory locations and (ii) applying a location signal to said control circuit representative of an address location being written to.

9. The apparatus as claimed in claim 8, wherein said control circuit is further configured to control said first and said second registers and said calculation circuit in response to said location signal.

10. The apparatus as claimed in claim 9, wherein said control circuit is further configured to instruct said calculate circuit to calculate said address in response to one of the following:

said X coordinate being written to a preselected one of said first and said second locations; and

said Y coordinate being written to a preselected one of said third and said fourth locations.

11. The apparatus as claimed in claim 1, further comprising:

a style table for storing data corresponding to a predetermined pattern for said pixel; and

a style counter for (i) indexing said data in said style table and (ii) generating a style data signal corresponding to said indexed data.

12. (CANCELED)

13. The apparatus as claimed in claim 11, wherein said style table is configured to store a non-repeating bit pattern up to a predetermined length for a drawing operation.

14. The apparatus as claimed in claim 11, wherein (i) a first register of said registers is memory mapped to a first location, a second location, a third location and a fourth location in said first address range and (ii) a second register of said registers is memory mapped to a fifth location, a sixth location, a seventh location and an eighth location in said first address range; and

said apparatus further comprising an address decoder for (i) monitoring said first to said eighth locations, (ii) generating a location signal representative of an address location being written to and (iii) indexing said style counter in response to said address location being written to.

15. An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register accessible via a bus for storing coordinates of a pixel to be drawn on said display;

a calculation circuit for calculating an address in a memory directly connected to said bus for storage of data corresponding to said pixel in response to said coordinates; and

a control circuit for controlling said register and said calculation circuit to cause said data to be stored in said memory across said bus by driving said address onto said bus, wherein said calculation circuit is configured to output said address in a first part and a second part, said first part comprising a word address corresponding to said address in said memory and representing a single memory word and said second part comprising a bit address representing a position of said pixel data within said single memory word.

16. The apparatus as claimed in claim 15, further comprising:

a second register for storing said pixel data in said single memory word prior to said single memory word being written to said address in said memory; and

a logic unit for writing data to said second register in dependence on said address calculated by said calculation circuit.

17. The apparatus as claimed in claim 16, wherein said logic unit combines data for at least two pixels to be drawn in dependence on said address of each of said pixel to permit storage of said data for said pixels in said single memory word.

18. The apparatus as claimed in claim 17, further comprising:

a comparator connected to said calculation circuit for (i) receiving said addresses, (ii) comparing said addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if said addresses are identical.

19. The apparatus as claimed in claim 18, wherein said control circuit is further configured to combine said data for said pixels in response to a receipt of said same address signal.

20. A method of generating a region of graphics on a display, the method comprising:

(A) storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

(B) storing a Y coordinate for said pixel in said first address range;

(C) calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates;

(D) controlling writing of said data across said bus into a memory directly connected to said bus by driving said address onto said bus; and

(E) memory mapping a first register storing said X coordinate to a first location and a second location in said first address range; and

(F) memory mapping a second register storing said Y coordinate to a third location and a fourth location in said first address range.

21. The method as claimed in claim 20, further comprising:

comparing said X and said Y coordinates with predetermined clipping limits; and

discarding said pixel data in response to at least one of said X and said Y coordinates exceeding said predetermined clipping limits.

22. (CANCELED)

23. The method as claimed in claim 22, further comprising:

monitoring said first, said second, said third and said fourth locations for a write.

24. The method as claimed in claim 23, further comprising:

calculating said address for said pixel in response to one of the following:

said X coordinate being written to a preselected one of said first and said second locations; and

said Y coordinate being written to a preselected one of said third and said fourth locations.

25. The method as claimed in claim 20, further comprising:

storing style data corresponding to a predetermined pattern for said pixel;

indexing said style data; and

generating a style data signal corresponding to said style data as indexed.

26. The method as claimed in claim 25, further comprising:

selecting a color for said pixel to be drawn in dependence on said style data signal.

27. The method as claimed in claim 20, further comprising:

storing said data in a single memory word prior to said single memory word being written to said address in said memory in dependence on the word address or a bit address.

28. The method as claimed in claim 20, further comprising:

combining data for at least two pixels to be drawn in dependence on a word address of each of said pixels to permit storage of said data for said pixels in a single memory word.

29. The method as claimed in claim 28, further comprising:

comparing said word address of consecutive pixels to be drawn; and

combining said data for said pixels if said word addresses are identical.

30. An apparatus for generating a region of graphics on a display, the apparatus comprising:

means for storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

means for storing a Y coordinate for said pixel in said first address range;

means for calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

means for controlling writing of said data across said bus into a memory directly connected to said bus by driving said address onto said bus.